Comp 331 – Today’s Overview
Intro to Electronic Circuits

1. Some Physical Background
2. Digital Circuits: Series and Parallel circuits
   • switch-resistor models
3. nFET and pFET transistors
4. CMOS gates

Physical Background
charge (coulombs)

voltage = joules/coulomb (V) volts
current (I) amperes
resistance (R) ohms
Ohm’s Law: V = IR
Power (Watts) \( P = VI = I^2R \)

Plinko Board model

Circuits
Electric vs. Electronic
Physical vs. Model
Digital vs. Analog

Electronic Components
Resistors (ohms)
Capacitors (capacitance (F) farads)

Input Devices
Output Devices (LED’s)
Printed Circuit Boards (PCB)
manufacturing process

Transistors as Switches
basic nFET and pFET models (source, gate, drain)
nFET: Vdd=closed  pFET: GND=closed

Digital Circuits
Series and Parallel switch/resistor models; Vdd & GND: LLV
(assert low) vs. LHV (assert high); duality or And’ing and Or’ing

Series Circuit: Fig 1. Parallel Circuit: Fig 2.

Transistors
manufacturing process; basic principles of operation (pn junctions)
Four Basic Rules for Building FET Circuits

- pFET sources must be connected to Vdd, nFET sources to GND
- Circuit output must be connected to Vdd via on a pFET or to GND via on an nFET
- Logic circuit output must never be connected to Vdd and GND at same time
- Circuit must use fewest number of FET’s

CMOS diagrams for NAND, NOR, AND, OR, and INV

Project 1 (Odd & Majority) : Implement on the BASYS2 Board the PLA circuit from Thursday

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
<th>odd</th>
<th>majority</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

odd \(\equiv (\neg a \& \neg b \& c) \land (\neg a \& b \& \neg c) \land (a \& b \& \neg c) \land (a \& b \& c)\)

majority \(\equiv (\neg a \& b \& c) \land (a \& b \& \neg c) \land (a \& b \& c)\)