Comp 331: Intro to Computer Hardware
Today’s Overview

1. Project_1A: Schematic Design of OddAndMajority circuit
2. Using the Aldec Active-HDL Simulator
3. Intro to VHDL - Project_1B: VHDL Design of OddAndMajority circuit

Project 1A (Odd&Majority): Implement on the BASYS2 Board the PLA circuit from last Thursday

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<th>odd</th>
<th>majority</th>
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odd \equiv (- a \& - b \& c)(- a \& b \& - c)(a \& - b \& - c)(a \& b \& c)
majority \equiv (- a \& b \& c)(a \& - b \& c)(a \& b \& - c)(a \& b \& c)

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Functional Simulation Options

Setting Functional Simulation Signals
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity OddAndMajority is
    port(           
a : in STD_LOGIC;
b : in STD_LOGIC;
c : in STD_LOGIC;
Odd : out STD_LOGIC;
Maj : out STD_LOGIC
    );
end OddAndMajority;

architecture OddAndMajority of OddAndMajority is
begin
    Odd <= (not a and not b and c) or (not a and b and not c) or (a and not b and not c) or (a and b and c);
    Maj <= (not a and b and c) or (a and not b and c) or (a and b and not c) or (a and b and c);
end OddAndMajority;

architecture OddAndMajority_top of OddAndMajority_top is
    component OddAndMajority
        port(           
a : in STD_LOGIC;
b : in STD_LOGIC;
c : in STD_LOGIC;
Odd : out STD_LOGIC;
Maj : out STD_LOGIC
        );
    end component;
    -- for all: OddAndMajority use ...
    begin
        C1 : OddAndMajority
            port map(
                a => sw(0),
b => sw(1),
c => sw(2),
Odd => ld(0),
Maj => ld(1)
            );
    end OddAndMajority_top;