Comp 331: Intro to Computer Hardware
Today's Overview

1. Combinatorial Logic
2. n-input Multiplexers
   - 2-to-1 MUX
   - 4-to-1 MUX
   - Quad 2-to1 MUX
   - VHDL implementations
3. VHDL Statements (to be continued)
   - if statement
   - procedural/sequential stats; process block
   - case statement
4. Generic statements

Combinatorial Logic Circuits:
output is function of current inputs only

Sequential Logic Circuits:
output depends on current inputs and past inputs

n-input Multiplexer: n-way digital switch that switches one of n inputs to the output

VHDL Example 2-to-1 MUX (logic equation)
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity mux21a is
port (a : in STD_LOGIC;
b : in STD_LOGIC;
s : in STD_LOGIC;
y : out STD_LOGIC);
end mux21a;

architecture mux21a of max21a is
begin
  y <= (not s and a) or (s and b);
end mux21a;

VHDL Example 4-to-1 MUX (logic equation)
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity mux41b is
port (c : in STD_LOGIC_VECTOR(3 downto 0);
s : in STD_LOGIC_VECTOR(1 downto 0);
z : out STD_LOGIC);
end mux41b;

architecture mux41b of max41b is
begin
  z <= (not s(1) and not s(0) and c(0)) or (not s(1) and s(0) and c(1))
    or (    s(1) and not s(0) and c(2)) or (    s(1) and    s(0) and c(3));
end mux41b;
Quad 2-to-1 MUX (MUX2Way4)

VHDL Example : Quad 4-to1-MUX
Parallel Logic Example

```vhdl
entity mux24a is
case
port:
a : in STD_LOGIC_VECTOR(3 downto 0);
b : in STD_LOGIC_VECTOR(3 downto 0);
s : in STD_LOGIC;
y : out STD_LOGIC_VECTOR(3 downto 0);
end
architecture mux24a of mux24a is
begin
  s4 <= s & s & s & s;
y <= (not s4 and a) or (s4 and b);
end
end
```

Advanced VHDL
to be continued