1. Glitches
2. 7-Segment displays
3. 7-Segment Decoder
   - Karnaugh Maps to Logic Statements
   - Case Statement
4. hex7seg.vhd

Glitch: output is momentarily 0 when it should be 1 or momentarily 1 when it should be 0.

Example

Implement and simulate the above (see Fig 5.17)
Print out copies .vhd code and simulation run

Overview of LED and 7-Segment Displays

How LED’s work

if V2 > V1 on; if V2 ≤ V1 off

Two ways I/O pins of FPGA’s turn on LEDs
either V2 = Vdd and gate V1 to GND (7 seg. display; 0 -> on)
or V1 = GND and gate V2 to Vdd (LED’s ld7 – ld0; 1 -> on)

7 Segment display arrangement: “bars” a – g (next slide)
Common anode vs. common cathode “flavors”-

Implementing a 7-segment display

Logic implementation based on Karnaugh maps
(hex7seg_le)

Karnaugh Map
For 'e' segment

Segment Values

Note: with common anode
Display: 0 = on; 1 = off
In Class Exercise: Example 13

Implement on the BASYS-2 board hex7segb.vhd.

Print out copies of .vhd files and demonstrate your BASYS-2 board implementation