10/02/2012

Comp 331: Intro to Computer Hardware
Today's Overview

A 1-Bit Comparator
A 1-Bit Comparator with Carry In/Carry Out
Cascading 1-Bit Comparators
VHDL Procedures
Relational Operators in VHDL
Building and Implementing a 4-Bit Comparator

A 1-bit Comparator

A 2-bit Comparator

x | y | < | = | >  
---+---++---+---+---
0 | 0 || 0 | 1 | 0  
0 | 1 || 1 | 0 | 0  
1 | 0 || 0 | 0 | 1  
1 | 1 || 0 | 1 | 0  

x | y | < | = | >  
---+---++---+---+---
00 | 00 || 0 | 1 | 0  
00 | 01 || 1 | 0 | 0  
00 | 10 || 0 | 0 | 1  
00 | 11 || 0 | 0 | 1  
01 | 00 || 1 | 1 | 0  
01 | 01 || 1 | 1 | 0  
01 | 10 || 1 | 0 | 0  
01 | 11 || 1 | 0 | 0  
10 | 00 || 0 | 1 | 0  
10 | 01 || 0 | 0 | 1  
10 | 10 || 0 | 0 | 1  
10 | 11 || 0 | 0 | 1

XOR Equations for 1-Bit Comparator

Gout <= (x > y) or ((x = y) and Gin = 1))
Eout <= (x = y) and (Gin = 0) and (Lin = 0)
Lout <= (x < y ) or ((x = y) and (Lin = 1))

Gout <= (x and not y) or (x xor y) and Gin
Eout <= (not x and not y  and not Gin and not Lin) or (x and y and not Gin and not Lin)
Lout <= (not x and y ) or (not x and Lin) or (y and Lin)

Exercise 1: A 4-Bit Cascaded Comparator
Project Example20a

Design a 4-bit cascaded comparator using four instantiations of the comp1bit.vhd component that compares x(3:0) with y(3:0).

Call the file comp4a.vhd (see next slide)

Using comp4a design a second "top" program comp4a_top 
(similar to Listing 5.3.1) that implements comp4a on a BASYS-2 board.

Note: ld(2) is lt, ld(1) is eq and ld(0) is gt

Instructor Check: _____

Comp 331 – Intro to Hardware Comparators

A 1-bit Comparator

x | y | < | = | >  
---+---++---+---+---
00 | 00 || 0 | 1 | 0  
00 | 01 || 1 | 0 | 0  
00 | 10 || 0 | 0 | 1  
00 | 11 || 0 | 0 | 1  
01 | 00 || 1 | 1 | 0  
01 | 01 || 1 | 1 | 0  
01 | 10 || 1 | 0 | 0  
01 | 11 || 1 | 0 | 0  
10 | 00 || 0 | 1 | 0  
10 | 01 || 0 | 0 | 1  
10 | 10 || 0 | 0 | 1  
10 | 11 || 0 | 0 | 1

A 2-bit Comparator

Gout <= (x > y) or ((x = y) and Gin = 1))
Eout <= (x = y) and (Gin = 0) and (Lin = 0)
Lout <= (x < y ) or ((x = y) and (Lin = 1))

Gout <= (x and not y) or (x xor y) and Gin
Eout <= (not x and not y  and not Gin and not Lin) or (x and y and not Gin and not Lin)
Lout <= (not x and y ) or (not x and Lin) or (y and Lin)

Comp1bit.vhd

entity comp1bit is
port (x : in STD_LOGIC;
y: in STD_LOGIC;
Gin: in STD_LOGIC;
Lin: in STD_LOGIC;
Gout: out STD_LOGIC;
Eout: out STD_LOGIC;
Lout: out STD_LOGIC);
end comp1bit;
architecture comp1bit of comp1bit is
begin
Gout <= (x and not y) or (x and Gin) or (not y and Gin);  
Eout <= (not x and not y and not Gin and not Lin) or  
(not x and y) and not Gin and not Lin);  
Lout <= (not x and y) or (not x and Lin) or (y and Lin);
end comp1bit;
Example 20a – A 4-bit Comparator using four Cascaded 1-bit Comparators

entity comp4a is
  port(
    x: in STD_LOGIC_VECTOR(3 downto 0);
    y: in STD_LOGIC_VECTOR(3 downto 0);
    lt: out STD_LOGIC;
    eq: out STD_LOGIC;
    gt: out STD_LOGIC
  );
end comp4a;

architecture comp4a of comp4a is
  begin
    four instantiations of the comp1bit component
    ...
  end comp4a;

Declaring VHDL Functions and Procedures

function identifier (parameter_list) return type is
  begin
  ...
end function;

procedure identifier (parameter_list) is
  begin
  ...
end procedure;

Comp1bit as a Procedure (Details from Listing 5.30)

use IEEE.STD_LOGIC_unsigned.all;

procedure comp1bit (
  x: in std_logic;
  y: in std_logic;
  Gin: in std_logic;
  Lin: in std_logic;
  Gout: out std_logic;
  Lout: out std_logic;
  Eout: out std_logic)
  is
  Gout := (x and not y) or (x and Gin) or (not y and Gin);
  Lout := (not x and not y and not Gin and not Lin) or
    (x and y and not Gin and not Lin) or
    (y and Lin);
end procedure;

N-bit comparator (generic)

entity comp is
  generic (N: integer := 0);
  port(
    x: in STD_LOGIC_VECTOR(N-1 downto 0);
    y: in STD_LOGIC_VECTOR(N-1 downto 0);
    gt: out STD_LOGIC;
    eq: out STD_LOGIC;
    lt: out STD_LOGIC)
end comp;

architecture comp of comp is
  begin
    process(x, y)
    begin
      if (x > y) then
        gt <= '1';
      elsif (x = y) then
        eq <= '1';
      elsif (x < y) then
        lt <= '1';
      end if;
    end process;
  end comp;

Exercise 2: Project Example20b

Implement Listing 5.30 comp4.vhd and Listing 5.31 comp4b_top.vhd for the BASYS-2 board

Instructor check ___

Exercise 1

Project: Example 20a
1. compbit.vhd
2. comp4a.vhd
3. comp4a_top.vhd
Instructor Check: ___

Exercise 2

Project: Example 20b
1. compbit.vhd
2. comp4b.vhd
3. comp4b_top.vhd
Instructor Check: ___

Corrections to 5.30
missing E(0) = '0';