Comp 331: Intro to Hardware
Datapaths and Control Units

Library IEEE;
use IEEE_STD_LOGIC_1164.all;
use IEEE_STDLOGIC_UNSIGNED.all;

entity gcd1 is
  port(x : in STD_LOGIC_VECTOR(3 downto 0);
y : in STD_LOGIC_VECTOR(3 downto 0);
gcd : out STD_LOGIC_VECTOR(3 downto 0));
End gcd1;

architecture gcd1 of gcd1 is
begin
  process(x,y)
  variable xv, yv :STD_LOGIC_VECTOR(3 downto 0);
  begin
    xv := x;
yv := y;
    while (xv /= yv) loop
      if xv < yv then
        yv := yv – xv;
      else
        xv := xv – yv;
      end if
    end loop
    gcd <= xv;
  end process;
end gcd1;

Creating a Datapath

Registers
  draw register boxes with appropriate input and output and clr,
  clk & load signals

Arithmetic & Logic Units
  define appropriate combinatorial blocks

Make Connections between registers and combinatorial blocks

Creating the Control Path – A FSM

Exercise – Do Example 63: gcd1 implementing the
circuit on the BASYS-2 board.

Listing 9.2 – Data Path (use generic mux2g from
Example 10 and register from Example 44)
Listing 9.3 – Control Path
Listing 9.4 – combines data & control paths
Listing 9.5 – gcd1_top (using clkdiv and x7segbc components)