Part 1: Project Setup – same
Part 2: Design Entry – gates2.bde

Click on BDE
The next two screens are straight-forward
Enter gates2

Click [new], select Port direction in and type: a. Do the same for input b
Next select Port direction out and type: and_gate, nand_gate, or_gate, nor_gate, xor_gate, and xnor_gate
Click [Finish]
This will generate a block diagram (schematic) template with input and output ports. You will have to select and drag the components so they all fit on one screen.

Click on the Show Symbols Toolbox icon to display the gate symbols. Use the pull down menu to see the list of gates; The corresponding gate symbol will appear below.
Selecting from the pull down menu, click and drag the corresponding gate symbol positioning it where needed.

Wiring comes next
Select the wire tool.

First connect the input of the output ports to the outputs of the corresponding gates.

Next wire the inputs of the and gate to the outputs of the input ports a and b.

Next “drop” wires from the previously created wires; these will be used to connect the outputs of input ports a and b to the inputs of the other five gates.

Note that wires are horizontal or vertical can be created between any two grid points.

Finally right click on gates2.bde and from the pull down menu compile your schematic.
Part 3: Simulation

From Design Flow click on functional simulation options
Click on the Select Design Files Icon to open window below
Select gates2.bde and add it to the list on the right. Click [ok]

Choose Top-Level Unit to open the following menu

Select gates2 and Add. Click [ok]
Finally Check Use Default Waveform. Click [ok]
This should open a Simulation window. Right click the two input signals a and b and select the Simulators option.
Select the Clock option and set the Frequency for a to 50MHz. Click [Apply]

Repeat for input signal b but set the frequency to 25MHz (slower). Click [Apply]
Run the simulation for 100 ns (default).

When done stop (or reset) the Simulation.

If your design is correct it should match the above.
Part 4: Top-level Design: Design Entry – gates2_top.bde

To implement the circuit on the BASYS-2 board create a separate top-level design in which the inputs and outputs are the switches, buttons, LED’s etc. of the BASYS-2 board.

Click on BDE
Create another block diagram schematic called gates2_top whose inputs are sw[1:0] (which will correspond to switches 0 and 1 on the BASYS-2 boards) and whose outputs are ld[5:0] (which will correspond to LED’s 0 thru 5)
The block diagram (schematic) has signal vectors (arrays of signals) for the input and output ports which are buses (like arrays of wires). The thicker lines denote buses not wires.

Also note that clicking the Show Symbols Toolbox icon will display a block symbol for gates2s. Click and drags this unit symbol into your diagram.
Now to make connections we need the bus tool first. Close the Symbols Toolbox to see it (alternately you can click on the [>>] icon)
The bus tool works like the wire tool. Make a bus leading off the input port and a bus into the output port.
Use the wire tool to connect the inputs and output from the gate2 block to the buses.

However we need to identify each wire with a bus wire. We do this using a naming convention. The two wires making up the sw bus are labeled sw(0) and sw(1); the six wires making up the bus leading into the ld bus are called ld(0), ld(1), … ld(5).

Right click on each wire to open up a menu window which will allow you to name that wire.
Right clicking on the wire leading from and-gate will open up the following window. Enter `ld(5)` in the segment text box. [Click [ok]. Repeat for the other wires. See the next diagram to get the naming correct!
If you did the wiring correctly – you should see this
Now select gates2_top and compile.
Part 5: Synthesis and Implementation

From Design Flow click on synthesis | reports.

Make sure the following information correctly appears

Top-level Unit: gates2_top
Family: Xilinx 13x SPARTAN3E
Device: 3s100ecp132

Click [Ok]

When done form the Design Flow window click on synthesis. A window will open. When done close the window. This assumes there are no errors
From the Design Flow window click on implementation | options.

Main tab:

Make sure the device is **3s100ecp132**

Constraint file should be **Custom constraint file**

Browse to find **basys2board.ucf**
Translate Tab: Allow Unmatched LOC Constraints
Bit Stream Tab: Uncheck Do Not Run Bitgen.
Startup Options Tab: Select JTAG Clock. Click [ok]
From the Design Flow window click **implementation**. If successful you should see the follow.
Part 6: Programming the FPGA Board

Plug in your BASYS-2 board and turn it on. Fire up Digilent Adept.

Browse to find the gate2_top bit file (Example2\gates2\implement\ver1\rev1\gates2_top.bit) and click on [Program] to download the bit file to your board.

Test that your circuit performs correctly

\[
\begin{align*}
ld(5) &= sw(1) \text{ and } sw(0); & ld(4) &= sw(1) \text{ nand } sw(0) \\
ld(3) &= sw(1) \text{ nor } sw(0); & ld(2) &= sw(1) \text{ or } sw(0) \\
ld(1) &= sw(1) \text{ xnor } sw(0); & ld(0) &= sw(1) \text{ xor } sw(0)
\end{align*}
\]